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SUPER LOW-NOISE HEMTs WITH A T-SHAPED GATE STRUCTURE

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Abstract

The low noise property of HEMTs was studied, based on the noise power generated in the devices. 0.5 μm- and 0.25 μm-gate HEMTs were fabricated, to study the noise power generated in the intrinsic region of the devices. In order to leave the extrinsic noise power out of consideration, a T-shaped gate structure was developed to make equal the gate-resistances of these devices. It was shown that the noise power was independent of frequency and strongly dependent on the gate length. The resultant quarter micron gate HEMTs achieved the noise figures of 1.0 dB at room temperature and 0.5 dB at 100K at 20 GHz.

Introduction

Recently, it has been accepted that HEMTs exhibit superior low noise performance, as compared with GaAs MESFETs 1), 2). Low-noise HEMTs have proved their worth in applications such as satellite communication systems and radio astronomical observatories 3), 4).

However, it is not quite clear why HEMTs have the superior low noise properties. In this paper, we are trying to clarify the reason.

Generally, the empirical equation given by Fukui is used to describe the relation between the noise figure and the device parameters 5). But the physical meaning of the fitting parameter K_f in the equation is obscure, therefore this equation cannot be always effective for the analysis of the noise property. Then we will start at the definition of the noise figure.

$$F = 1 + \frac{P_n}{G_{as} \cdot kT_o} \qquad (1)$$

where G_{as} is the associated gain, kT_o*(T_o = 290K, k : the Boltzmann constant) is the available output noise power of a resistor at 290K, P_n is the noise power generated in the device. Our attention will be focused on the noise power Pn, instead of on the noise figure.

The source of the noise power generated in the device can be divided into two parts. One is the intrinsic region of FETs and the other is the extrinsic elements, R_g, R_s. In order to investigate the essential noise property of HEMTs, we consider the noise power generated in the intrinsic region. So we study the dependence of noise power on the gate length, using devices having the same gate-resistance and the same source-resistance. It is difficult for a conventional quarter micron gate structure to have the same gate-resistance as a half micron gate structure. So we developed HEMTs with a T-shaped quarter micron gate structure in which the gate cross-section is large enough. Using the completed devices, we discuss the noise property as compared with that of the half micron gate devices.

Device fabrication

Figure 1 shows the fabrication process for T-shaped gate HEMTs. 1) A quarter micron gate pattern is defined, and the insulator film on the wafer is dry-etched. 2) After the gate metals are evaporated, the photoresist pattern is aligned to the quarter micron gate in order to obtain the T-shaped gate structure. 3) The evaporated metals are

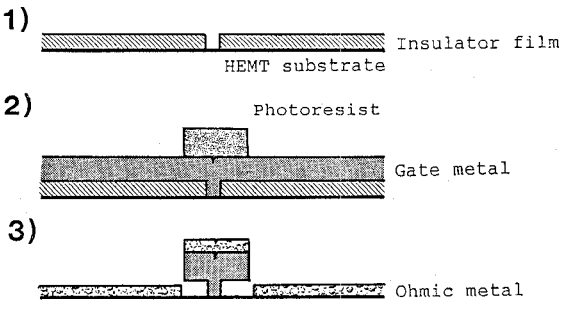

Fig. 1 Major steps in the fabrication process.

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etched off by Ar^+ ion milling, and the insulator film is removed by wet-etching. Finally, the evaporated AuGe/Ni/Au are alloyed to make the source- and drain-ohmic contacts. The alloy-temperature is low enough to keep the gate Schottky contact, but a low ohmic contact resistance in the range from 0.1 to 0.2 ohm-mm is obtained. The structure of the epitaxial wafer used here is the same as that previously reported 6).

The total gate widths in the two types of completed devices are 100 μm and 200 μm, respectively. Figure 2 is a photograph of the fabricated chip(W_g = 100 μm). The unit gate width is a quarter of the total gate width. The length of the top layer in the T-shaped gate is 1.0 μm, which defines the separation between the source- and drain-electrodes. The SEM view of the gate region is shown in Fig. 3.

Microwave performance

Figure 4 shows the noise figure F and the associated gain G_{as} versus the drain current of a quarter micron gate HEMT(W_g = 100 μm) at a drain voltage of 3 V. The lowest noise figure F_o and the associated gain G_{as} obtained were 1.0 dB and 8.2 dB at 20 GHz at room temperature. Figure 5 shows the optimum noise figure and associated gain versus the frequency as a parameter of the total gate width. At 12 GHz, the optimum noise figure and the associated gain respectively were 0.7 dB and 10.4 dB, and at 30 GHz they were 1.7 dB and 6.1 dB at room temperature.

The temperature dependence of the noise figure and the associated gain are shown in Fig. 6. The noise performance is strongly dependent on the temperature, the lowest noise figure of 0.5 dB and the associated gain of 8.8 dB were achieved at 20 GHz at 100K.

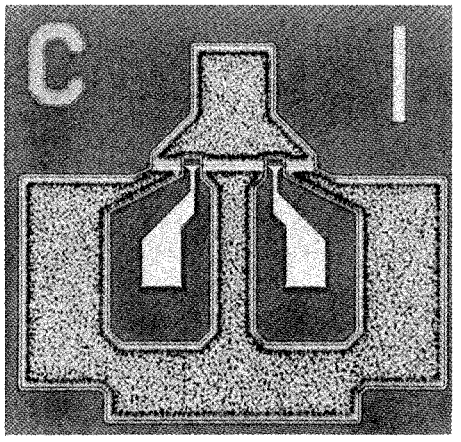


Fig. 2 Photograph of the fabricated HEMT chip.

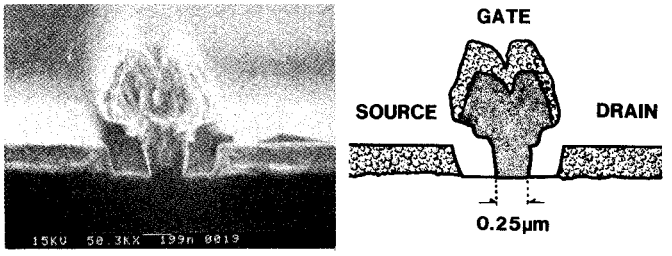


Fig. 3 SEM micrograph and schematic illustration of the gate cross-section.

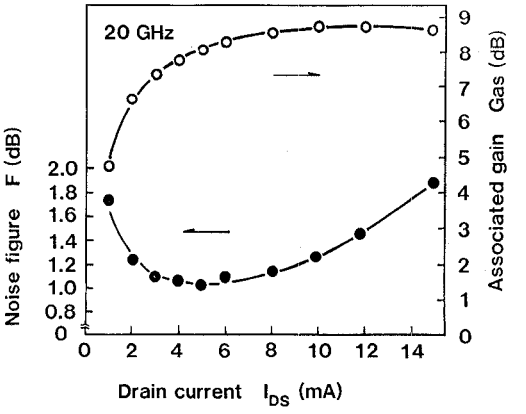


Fig. 4 Noise figure and associated gain as a function of the drain current.

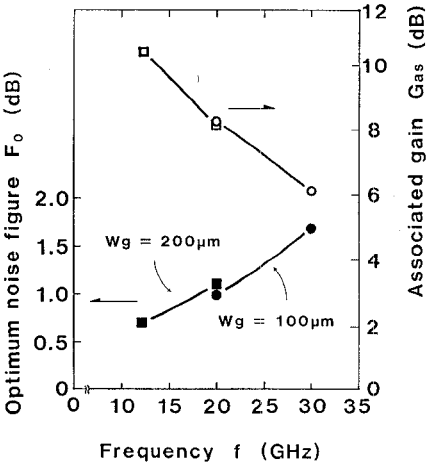


Fig. 5 Optimum noise figure and associated gain versus frequency.

Figure 7 shows the distribution of the measured noise figures at 20 GHz. The mean value was 1.1 dB and the standard deviation was 0.05 dB.

Figures 8(a) and (b) show the equivalent circuits of the two types of HEMTs, in which the gate lengths are a half micron and a quarter micron, respectively. These values were derived from measured S-parameters, except for gate resistance, which were estimated from DC measurements 5). The devices were biased at a drain voltage of 2 V and a drain current of 10 mA. Note that in spite of the different gate lengths, the gate-resistances and the source-resistances of the different devices are roughly equal. Due to the T-shaped gate structure, the gate resistance is low, such as 0.3 ohms.

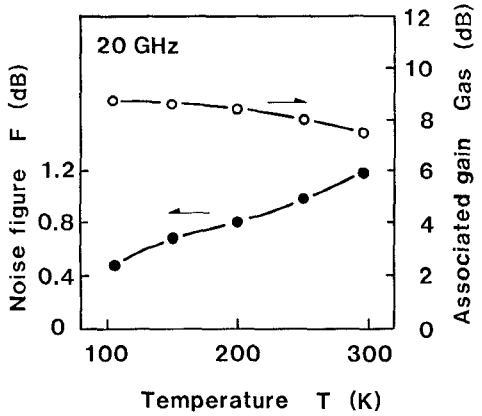


Fig. 6 Noise figure and associated gain as a function of the temperature (V_{DS} = 2 V, I_{DS} = 2.5 mA, W_g = 100 μm).

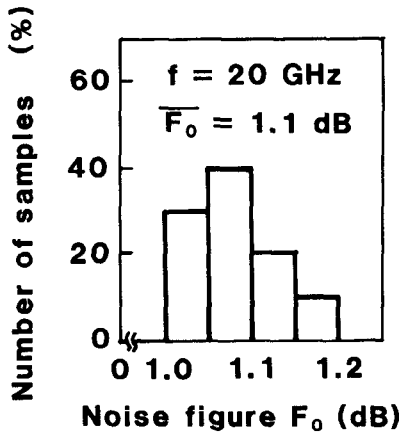
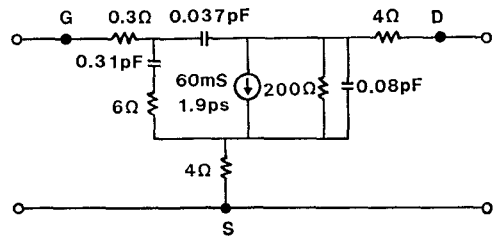
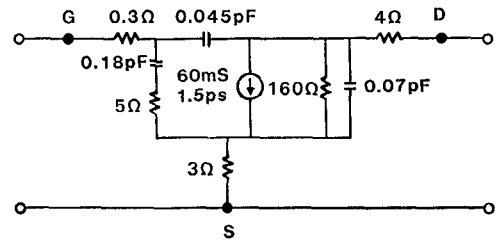


Fig. 7 The distribution of the noise figure.

The unity current gain cut-off frequency, which is obtained by extrapolating the $|H_{21}|$ value based on the relation to be inversely proportional to the frequency, is 43 GHz at a drain current of 5 mA for the quarter micron gate HEMTs(W_g = 100 μm).



(a) L_g = 0.5 μm



(b) L_g = 0.25 μm

Fig. 8 Equivalent circuits of the two types of HEMTs (W_g = 200 μm).

Discussion

Figure 9 is the chart (F-G chart) representing the relation between the noise figure and the associated gain based on the equation (1). Using this chart, it is easy to discuss the noise power P_n generated in the device. The solid lines show the relation between the noise figure F and the associated gain G_{as} when the noise power P_n generated in the device is constant. The parameter is P_n/kT_o. Curve A shows the increase in the noise figure with the decrease in the associated gain when the noise power is constant(ex. P_n/kT_o = 2). Line B shows that the noise figure is constant when the noise power is proportional to the associated gain. This corresponds to the case where the source of the noise power exists solely in the input portion of the device. The noise figure improves along line C, when the noise power decreases and the associated gain is constant.

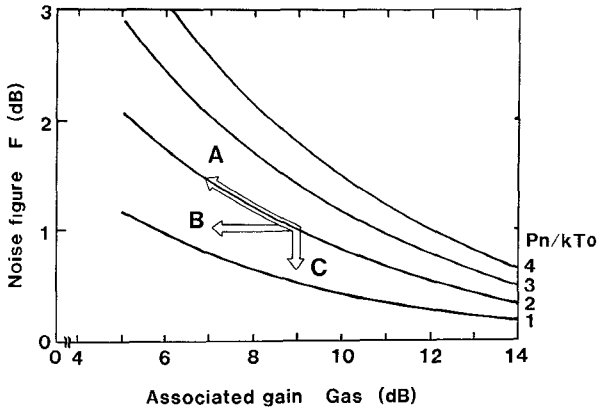


Fig. 9 Relation between noise figure and associated gain as a parameter of the noise power (F-G chart).

Figure 10 shows the plots of the property of the completed devices(L_g = 0.5, 0.25 μm) on an F-G chart. This figure shows the following;

1. The noise figure of each device increases along the curves of the constant noise power with the frequency. The noise power is insensitive to the frequency in the range from 12 to 30 GHz.
2. The noise power is independent of the associated gain. According to the discussion on the line B, we think the parasitic resistance generates less noise power than the intrinsic region of the device.
3. The noise power P_n is strongly dependent on the gate length, and the noise power of the quarter micron gate HEMTs decreases by 40 % as compared with that of the half micron gate HEMTs.

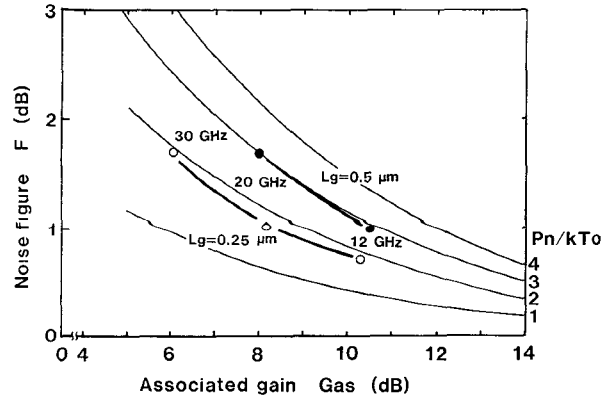


Fig. 10 Optimum noise figure and associated gain of the fabricated HEMTs on the F-G chart.

It can be concluded from the results stated above that the noise power in the devices fabricated here mainly originates in the intrinsic region. We think this is the first step toward making clear the reason why HEMTs have superior low noise property.

Summary

A T-shaped gate structure to reduce the gate resistance of quarter micron HEMTs has been developed. At room temperature, HEMTs achieved the noise figure of 1.0 dB at 20 GHz. It was shown that our attention to the noise power was effective to discuss the noise property of the devices. The noise power of our quarter micron HEMTs decreased by 40 % as compared with that of our half micron HEMTs.

Acknowledgment

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*) The noise power should be defined by "kT·Δf", but it is represented by "kT" in this paper.